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FMM and NDC technology-independent finite-memory nonlinear device models: ADS implementation and large-signal validation results

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Abstract

Recently proposed, general-purpose mathematical approaches, such as the Finite Memory Model (FMM) [6] and the Non-linear Discrete Convolution Model (NDC) [7], are used for the nonlinear modeling of electron devices. Both models derive from the same theoretical approach and are identified on the basis of conventional DC (and/or pulsed characteristics) and small-signal differential parameter measurements.
The implementation of the two models in the framework of the Agilent-ADS CAD package is described in the paper and a wide experimental validation, including small- and large-signal results, is presented for GaAs-MESFET, and PHEMT devices.

INTRODUCTION

In the last few years a number of mathematical approaches [1][2][3] have been proposed for the look-up-table based nonlinear modeling of electron devices. The basic aim of these methods is that of providing accurate large-signal performance prediction directly in terms of commonly available experimental data (i.e., DC or pulsed current characteristics and bias dependent AC small-signal measurements), without the need for equivalent circuits and technology-dependent analytical functions to describe the nonlinear device characteristics.
The recently proposed FMM [6] and NDC [7] empirical models follow this kind of approach. In particular, they are purely mathematical, nonlinear integral models, where the duration of memory effects in the intrinsic device is forced to be finite.
After a review of the finite memory nonlinear modeling approach, two different ways for its implementation in the framework of commercially available CAD-tools are described, leading to the Finite Memory Model (FMM) and to the Nonlinear Discrete Convolution (NDC) Model formulations. In particular, details on the implementation in the Agilent ADS CAD-tool are given in the paper. A section dedicated to experimental validation, including small- and large-signal results for different devices, concludes the paper.

THE FINITE MEMORY MODELING APPROACH

Finite memory modeling concepts are briefly recalled in this section (see Ref.[1],[6],[7] for a detailed discussion). A purely mathematical functional description of the intrinsic device nonlinear dynamics is adopted, where the instantaneous currents depend on both "present" and "past" values of the voltages. This kind of description can be simplified by assuming that the functional relation between currents and voltages only involves memory effects which are short in relation with the typical operating frequencies of the device. The validity of such an hypothesis has been verified by considering both accurate two-dimensional numerical simulations and actual measurements on devices not affected by strong parasitics and/or important low-frequency dispersive phenomena. In the general case, phenomena involving *slow* dynamic effects in comparison with the intrinsic device must be modeled apart. More precisely, low-frequency dispersive phenomena can be taken into account by introducing an additional dependence of the instantaneous currents on a set of state variables [5] (related to the mean values $\underline{V_0}$ of the applied voltages and possibly to P_0 when dispersion also derives from self-heating). Moreover, important parasitics can be described by means of series linear lumped elements as shown in Fig.1, where also a linear parallel parasitic network has been considered.
Under these assumptions a finite-memory description, T_M being the memory time duration, can be adopted without introducing important approximations of the device dynamics. For example, by considering a single

port device (multiport formulation is obtained by interpreting the following equations in vector form), we have [1]:

$$i(t) = \psi \left| v(t-\tau), V_0 \right|_{\tau=0}^{\tau=T_M} . \tag{1}$$

Relation (1) between current and voltage of the intrinsic device can be conveniently simplified in order to allow a feasible model identification. In fact, the functional description can be linearised with respect to suitably defined voltage deviations $e(t,\tau) \doteq v(t-\tau) - v(t)$, since these keep small under short memory conditions (i.e., small T_M) even in the presence of large voltage amplitudes. Linearisation leads to the following expression:

$$i(t) = F_{LF}[v(t), V_0] + \int_0^{T_M} g[v(t), \tau]\ e(t,\tau)\ d\tau \tag{2}$$

where $F_{LF}[v(t), V_0]$ describes the device behaviour under static and dynamic operating conditions over a range of frequencies, which are low enough with respect to the intrinsic device RF dynamics, yet well above the cut-off of dispersive phenomena [2]; moreover, the second term in Eq.(2) represents a purely-dynamic single-fold convolution integral between voltage deviations and the "pulse response function" $g[\cdot]$, which is non-linearly controlled by the instantaneous applied voltage.

ADS IMPLEMENTATION

When considering discrete-spectrum signals, the voltage $v(t)$ can be described by a Fourier series as a sum of spectral components V_k, so that, according to well-known properties of the Fourier transform, eqn. (2) can be expressed, after simple mathematical developments, in the Harmonic-Balance-oriented form which represents the **FMM model formulation** [6]:

$$i(t) = F_{LF}[v(t), V_0] + \sum_{k=-\infty}^{+\infty} \widetilde{Y}[T_M, v(t), \omega_k] V_k e^{j\omega_k t} \tag{3}$$

where $\widetilde{Y}[\cdot]$ is a non-linearly voltage-controlled dynamic admittance, which only describes the purely dynamic phenomena under high-frequency operating conditions. This term is easily characterised by means of conventional DC and small-signal S-parameter measurements over a suitable grid of bias points and frequencies (see Ref.[6] for details on the identification procedure).

In order to make the implementation of the FMM expression (3) feasible in commercial CAD-tool environments, some approximations must be introduced. These mainly arise from the limitations of many CAD input interfaces for user-defined nonlinear models, which are mainly oriented to the implementation of "lumped-element" nonlinear equivalent circuits. In particular, ADS does not allow for nonlinearly controlled integral models but only for linear integral models or nonlinear models based on ordinary differential equations. Owing to these limitations, the dynamic admittance terms $\widetilde{Y}[T_M, v(t), \omega_k]$ must be conveniently approximated to comply with the CAD user-interface requirements. To this aim, a polynomial expansion of the $\widetilde{Y}[\cdot]$ function in the frequency domain can be adopted, so that the associated coefficients are simply algebraic nonlinear functions of the applied voltages. It is worth nothing that coefficient identification can be analytically conducted on a suitable grid of voltages by means of least-square minimisation of the deviations between the theoretical and approximated dynamic admittances [6], [8]. The polynomial expression can be finally implemented by using Symbolically-Defined Devices and Data Access Components (dataset variables). As well known, the SDD represents an N-port ADS circuit component where port currents are defined as a combination of nonlinear algebraic functions of port voltages, possibly followed by a frequency-dependent filtering, as shown in Fig.2. According to a suitable trade-off between accuracy and computational efficiency, a third order polynomial truncation was actually adopted, allowing the implementation of the dynamic admittances by means of three SDDs, one for each polynomial expansion term. Moreover, implementation of the $F_{LF}[\cdot]$ function was carried out by means of an additional SDD and proper low-pass filtering for the computation of the mean voltage values.

Alternatively, problems related to the approximation of the dynamic admittance can be also overcome by discretising Eq.(2) as a finite summation of "delayed" terms, leading to the **NDC model formulation** [7]:

$$i(t) = F_{LF}[v(t), V_0] + \sum_{p=1}^{N_D} g_p[v(t)]\ (v(t-p\Delta\tau) - v(t)) \tag{4}$$

where N_D is a suitably chosen number of "delay" intervals $\Delta\tau$, in which the memory has been divided. Eq.(4) describes the device dynamics by a non-linearly voltage controlled discrete convolution, where the $g_p[\cdot]$ functions

[1] It can be demonstrated that conventional quasi-static models are special cases of (1) with $T_M \to 0$.

[2] Low frequency dispersive phenomena can be reliably taken into account by means of different approaches [4], [5] involving the dependence of the F_{LF} function on the mean value V_0 of the applied voltage $v(t)$.

are purely algebraic and analytically identified starting from conventional AC small signal measurements [7]. This allows an easy implementation of the model, by directly using basic tools (nonlinear purely algebraic functions and delay operators are both available in SDDs) normally provided in CAD user-interfaces for the building of user-defined models. In particular, since one SDD is necessary for each current contribution corresponding to a single delay interval, a computational efficiency comparable with the FMM is obtained by limiting the summation to $N_D = 3$ terms.

EXPERIMENTAL VALIDATION

FMM and NDC model validation tests have been performed by means of ADS simulations both under small- and large-signal operating conditions. For example, Fig.3 shows the comparison between S-parameter measurements and simulations carried out with the FMM implementation for a power PHEMT device at the bias point $V_{GS} = -1.2V, V_{DS} = 6V$. Similar good agreement has been verified for a wide number of different bias points and, as expected, coherent results have been obtained by means of both the FMM and NDC formulations.
Single-tone validation tests under large-signal operating conditions have been carried out on the same PHEMT device. In particular, measurements and NDC-based gain predictions are presented in Fig.4 for a 50Ω-loaded power amplifier at the frequency of 5 GHz. Moreover, the first three harmonic components of the output power predicted by means of FMM are compared in Fig.5 with corresponding experimental data. As can be observed, accurate model predictions are obtained both under mild and relatively strong nonlinear operating conditions.
Finally, the modeling approaches have been applied in order to predict the intermodulation distorsion under double-tone large-signal operating conditions. Tab.1 shows, for instance, IMD results for a PHEMT-based power amplifier and in Tab. 2 conversion gain and third-order IMD are given for a 14 GHz, double-balanced cold-FET mixer based on four MESFET devices in shunt configuration [8], confirming that FMM and NDC models allow accurate predictions also for very critical large-signal mixing operations.

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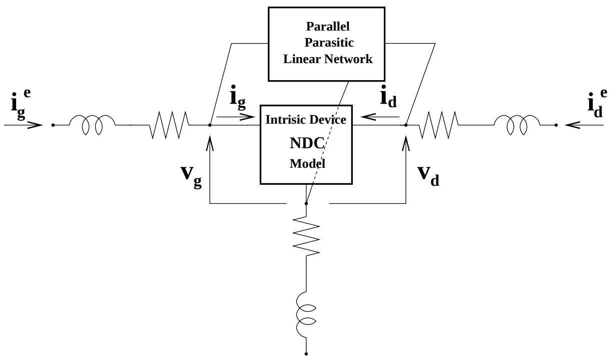

Figure 1: Equivalent scheme for the modeling of extrinsic parasitics in the FMM and NDC approaches.

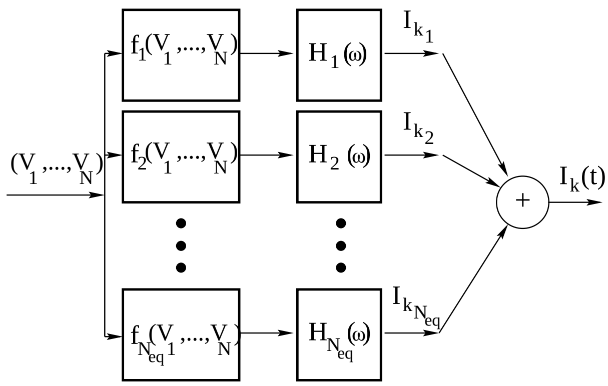

Figure 2: Evaluation of the instantaneous current at the $k-th$ SDD port by means of the applied voltages $V_1, V_2, ..., V_N$.

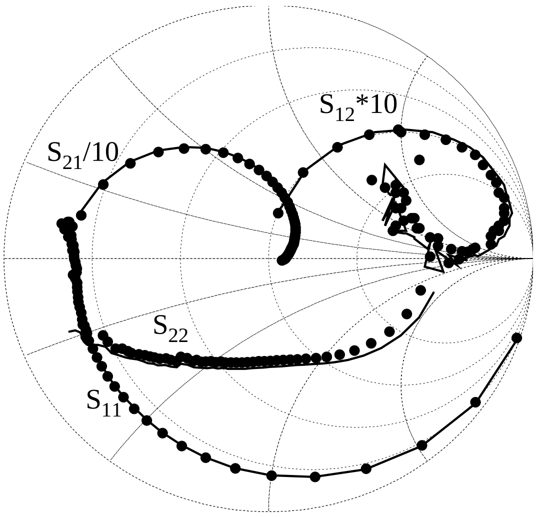

Figure 3: Comparison between S-parameters (1-50 GHz) measured (•) and simulated (−) through the FMM model for a power PHEMT device ($V_{GS} = -1.2\ V, V_{DS} = 6\ V$).

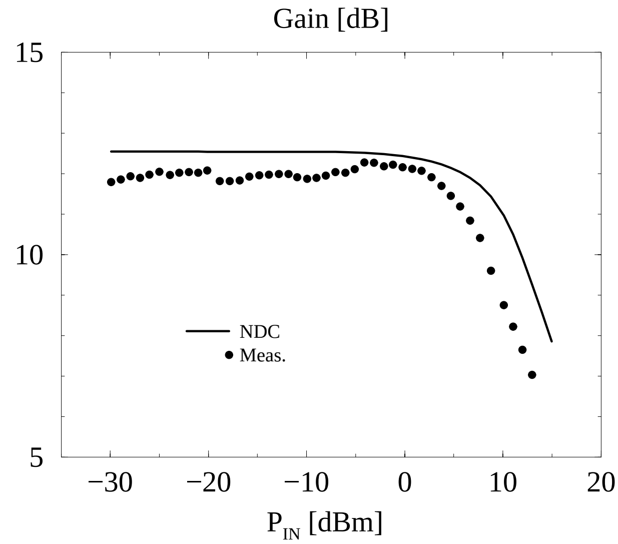

Figure 4: Measured (•) and predicted (NDC:−) gain for a power PHEMT device ($V_{GS} = -1.2\ V, V_{DS} = 6\ V, f = 5\ GHz$).

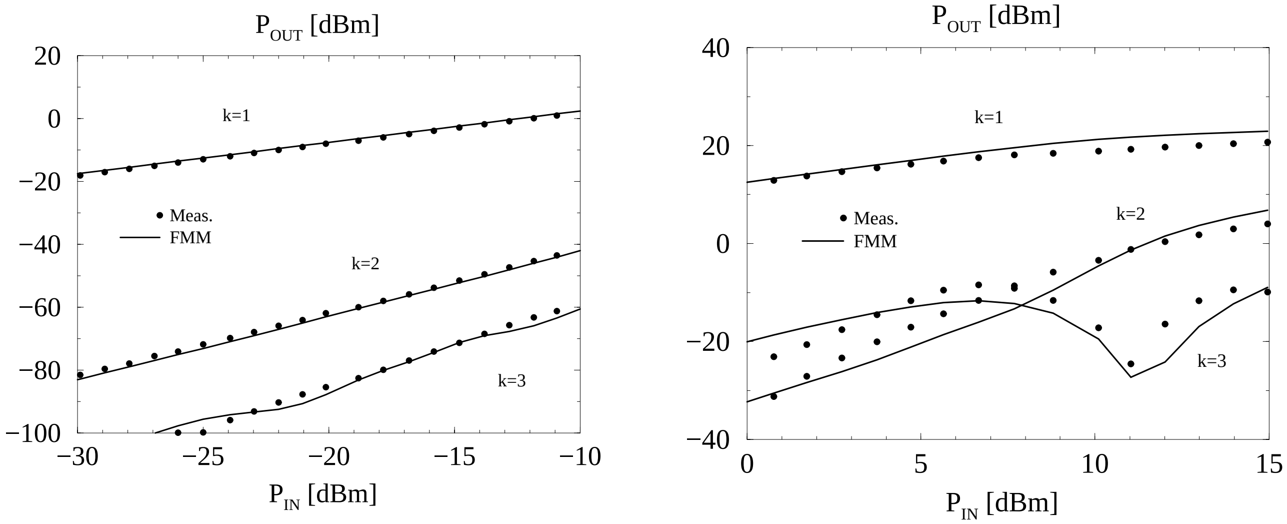

Figure 5: Measured (•) and predicted (FMM: −) output power associated to different harmonic components for a power PHEMT device ($V_{GS} = -1.2\ V, V_{DS} = 6\ V, f_1 = 5\ GHz$). Accurate model predictions are obtained both under mild (left) and relatively strong (right) nonlinear operating conditions.

	FMM (dBm)		MEAS. (dBm)	
P_{IN}(dBm)	P_{OUT}	P_{IM3}	P_{OUT}	P_{IM3}
−30	−17.3	−103.1	−17.5	−103.3
−25	−12.3	−92.7	−12.4	−89.4
−20	−7.3	−76.5	−7.6	−74.4
−15	−2.3	−60.8	−2.6	−59.3
−10	2.6	−46.5	2.4	−44.5

Table 1: Third-order intermodulation prediction by means of FMM at the frequency $2 \times f_2 - f_1$ ($f_1 = 4.995\ GHz$, $f_2 = 5.005\ GHz$) for a PHEMT-based power amplifier with 50 Ω source and load terminations ($V_{GS} = -1.5\ V, V_{DS} = 7\ V$). Identical power levels for the two RF tones were used.

	FMM model	NDC model	MEAS.
G_c	−8.5 dB	−8.5 dB	−8.6 dB
IMD_3	78.6 dBc	68.6 dBc	66.2 dBc
IP_3	10.8 dBm	5.8 dBm	4.5 dBm

Table 2: Intermodulation prediction for a 14 GHz double-balanced cold-FET mixer based on four MESFET devices, using both FMM and NDC (V_{GS}=V_P, P_{LO}=1dBm, P_{RF1}=P_{RF2}=-20dBm, f_{LO}=2GHz, f_{RF1}=13.99GHz, f_{RF2}=14.01GHz). G_C=Conversion Gain, IP_3=Third order intercept point.